z/OS Architectural Changes

Course Summary

Description

This course provides information relating to the changes brought about by z/OS and the z/architecture. It is intended for systems programmers migrating from OS/390 or moving to later releases of z/OS to bring themselves up to date regarding the changes these new releases bring.

Topics

- Z/Series architectural enhancements
- 64-bit Addressing
- Miscellaneous z/OS Enhancements

Audience

This course is designed for system programmers that need a better understanding of the architectural changes and operating system changes in the z/OS environment.

Prerequisites

There are no prerequisites for this class.

Duration

2-1/2 Day Sessions

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Course Outline

I. Z/Series architectural enhancements

A. Examine basic CPU architecture and the changes introduced in the z/990 & z/890 processor lines.
B. Introduce the considerations for additional processing engines, channel subsystems, and other configuration changes.
C. Discuss changes in system architecture because of 64-bit changes in registers, PSA, and the PSW.
D. Examine the tools and issues around CHPID mapping for the z/series processor.

II. 64-bit Addressing

A. Review virtual storage and DAT changes for 64-bit addressing
B. Examine new and expanded instructions for z/architecture.
C. Introduce services for using storage above the 2 GB bar.

III. Miscellaneous z/OS Enhancements

A. Examine basic WLM enhancements
B. Z/OS Velocity tool
C. WLM Initiator balancing
D. SDSF Enclave displays
E. Miscellaneous functions:
F. PAV for page data sets
G. TSO/E Broadcast data set changes
H. ASID resource relief
I. Workload Licensing